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Analysis of Low Voltage Level Shift Cascade Current Mirror

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Abstract: **The current mirror is one of the most basic building blocks both in analog and mixed mode VLSI circuits especially for active elements like as op-amps, current conveyors, current feedback amplifiers etc. At large supply voltages, there is a trade – off among speed, power and gain. The main characteristics under consideration are voltage, power, dynamic range, bandwidth, low offset voltage, high output voltage swing. The purpose of this work is to design a CMOS low power, low voltage current mirror with enhanced dynamic range. Most of the analog systems employ cascade current mirror & its various advancements. A low power low voltage cascade current mirror is designed, simulated and optimized to achieve required results. And a most recent current mirror architecture low voltage level shifted cascade current mirror is designed, simulated & optimized by using varying biasing voltages & currents and aspect ratio of transistor employed in current mirror. The Main emphasis in this work is focused to enhance dynamic range and to lower the power consumption.**

Keywords: **current mirror, voltage, power, dynamic range, power consumption.**

1. INTRODUCTION

Current mirror is an essential structure in most of the analog circuit applications, where the gain of the MOS can be expressed as product of its effective transconductance (g_m) and the output impedance (r_o). Due to continuous downscaling of MOS technology the device size is shrinking fast to enable higher unity gain frequencies. However, it reduces the gain of the MOS due to lowering of transconductance (g_m) and increase in output conductance ($1/r_o$) [1 & 2]. The speed and accuracy of analog circuit structures are determined by its settling behaviors. Fast settling demands high unity gain frequency and a single pole frequency response, whereas accurate settling requires high d.c. gain.

2. LOW VOLTAGE CMOS CURRENT MIRROR

One of the most fundamental building blocks of analog integrated circuit is the Low Voltage current mirror. Current mirror is enabling single current source to supply mirrors are output impedance and voltage headroom. The output impedance determines the variation of the mirrored current when the applied voltage varies. Higher output impedance implies less current variation with applied voltage and hence more stable current source Voltage headroom specifies how much voltage drop across the current mirror is required to operate the current mirror reliably. This is especially important for low voltage circuit design. The low voltage cascade current mirror is shown in figure 2.1. We assume that the current mirror transistors M1 and M2 have identical, aspect ratio. $A_M = \frac{W1}{L1} = \frac{W2}{L2}$ Where W1 and W2 are the transistor channel width and L1 and L2 are the transistor length.

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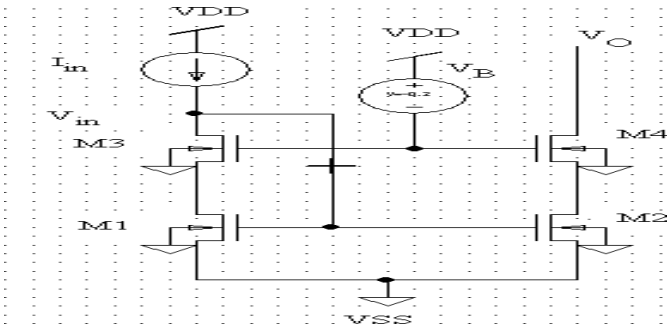

Figure 2.1 Low Voltage Current Mirror

Similarly, the transistor M3 and M4 are assumed the same aspect ratio $A_C = \frac{W3}{L3} = \frac{W4}{L4}$.The aspect ratio A_M may be different from the aspect ratio A_C. In the analysis of the dynamic range the same aspect ratio of A_M and A_C and we use standard Schman –Hodges transistor model for the transistor in the saturation region and we neglected the bulk effect and assume that all the NMOS transistors have the identical. Low voltage current mirror input current I_{in} find the gate- source voltages and drain -source voltages

$$V_{GS1} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}} \quad (2.1)$$

Gate to source voltage of transistor M3

$$V_{GS3} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_C}} \quad (2.2)$$

Drain to source voltage of transistor M1 is

$$V_{DS1} = V_{BC} - Vtn - \sqrt{\frac{2I_{in}}{KA_C}} \quad (2.3)$$

$$V_{DS3} = V_{GS1} - V_{DS1} = 2V_{tn} - V_{BC} + \sqrt{\frac{2I_{in}}{K}}\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \quad (2.4)$$

Where, V_{tn} is the transistor threshold voltage,V_{BC} is the bias or gate voltage of transistor M3 and M4 and K is the transconductance parameter. Requiring $V_{GS} - V_{tn} \leq V_{DS}$ for both M1 and M3 result in:

$$\sqrt{\frac{2I_{in}}{K}}\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} + V_{tn} \geq V_B \quad (2.5)$$

Biasing voltage: $V_{tn} \leq V_B + \sqrt{\frac{2I_{in}}{KA_M}}$ (2.6)

In figure 2.1 low voltage current mirror, biasing voltage V_B is fixed when I_{in} increases, voltage of the gate –source voltage V_{GS3} of transistor M3 and V_{in} will increase, and voltage level at the drain terminal of M1 decreases. There by M1 enter the triode region which determine upper limit of I_{in}Below equation (2.7) ensure the saturation of M1 and determines the maximum value I_{in} for given value of the cascade bias voltage V_B we find $I_{in,max} = \frac{K}{2} A_M (V_{BC} - Vtn)^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2$ (2.7)

Equations (2.7) ensure the saturation of M3 and determine the minimum value of I_{in}. We find

$$I_{in,\,max} = \frac{K}{2} A_M (V_{BC} - 2Vtn)^2 \; A_M \quad (2.8)$$

Maximum value of the bias voltage even at the minimum value of input current equation (2.8) determine, and equation (2.8) determined the value of AC and AM which determined the saturation of M1 and the maximum value of input current. To ensure Saturation operation of transistors M1 and M3 the input current range determined by

$$\frac{K}{2} A_M (V_{BC} - 2Vtn)^2 \leq I_{in} \leq \frac{K}{2} A_M (V_{BC} - Vtn)^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \quad (2.9)$$

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In a practical design procedure equation (2.8) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3 even at the minimum value of input current, and equation (2.7) can then be used to determine values of A_C and A_M which will ensure saturation of M1, even at the maximum value of input current.

$$A_M \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \geq 2 I_{in,\max} \frac{2 I_{in,\max}}{V_T^2 K} \qquad (2.10)$$

Assuming as a typical case W1 = W3 and L1 = L3 i.e., identical aspect ratios for the mirror transistors and the cascade transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{2 I_{in,\max}}{V_T^2 K} \qquad (2.11)$$

In this case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} \qquad (2.12)$$

In this case the minimum output voltage of the current mirror is and is independent of the input current.

$$V_{out,\min} = V_B - V_{tn} = V_{tn} \qquad (2.13)$$

3. LEVEL SHIFTED CURRENT MIRROR

Level shifted current mirror operates at low voltage with the advantage of low input output voltage requirement, incorporates a level shifter PMOS transistor M5 (biased through a current I_{bias1}) at input port. For this structure, we have

$$V_{DS1}=V_{GS1}-V_{GS5} \qquad (3.1)$$

WhereV_{DS1}drain to source and V_{GS1} gate to source voltage of M1, V_{GS5} is the gate to source voltage of M5.

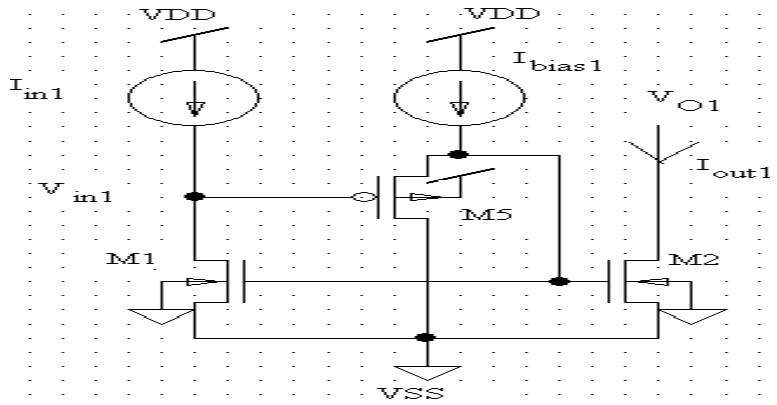

Figure 3.1 Level Shifted Current Mirror

A level shifted current mirror circuit structure is shown in figure 3.1 M3 is used to shift the voltage level at the drain terminal of M1. V_{in} a characteristics parameter of a low voltage current mirror and decides the range of input voltage swing in such circuits. The bias current (I_{bias1}) decides the operation region of M1. For example, low value I_{bias1} forces M3 to operate in sub threshold region I_{bias1} high I_{bias1} ensures M5 operates the triode region. For high value V_{DS2}, M2 operates in saturation region. Gate voltage of M1 is high correspondingly input current is also high. Thus, v_{in} can be calculated for this circuit structure if we know the values of V_{GS1} and V_{GS5} since $V_{tp} \geq V_{tp}$, there is a difficulty to keep the condition V_{GS1}- $V_{GS5} > 0$ valid in a level shifter-based circuit over a wide range of I_{in}. One of the solutions is to use a lateral p-n-p transistor for level shifting, and now V_{in}-V_{GS1}-$V_B > 0$ approximates as 0.7V and V_{GS1} is always more than 0.8v (if we assume V_{tn}=0.8v). As the device sizes are reducing and V_t is also reducing and there will be a situation where V_{GS1}-VB> 0 will not be valid and hence we may not be able to use p-n-p transistor.

4. LEVEL SHIFTED LOW VOLTAGE CASCADE CURRENT MIRROR

Figure 4.1 shown the level shifted low voltage cascade current mirror it is the combination of low voltage and level shifted current mirror and the combined the low voltage and level shifted current mirror present a level shifted low voltage current mirror. In this topology to achieve larger dynamic range for low voltage operation, the operation of M5 and M3 are similar

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in the figure 3.1 of M 5 and M1 we adopt the same assumptions in low voltage in this current mirror. We assume figure 3.1 the threshold voltage of M5 is V_{tp}, when the level shifted current mirror transistor M5 and M1 on must be conditions satisfied $V_{GS3} > V_{tn}$ and $V_{GS5} > V_{tp}$, but when $V_{tp} > V_{tn}$ there is a difficulty to the condition satisfy $V_{DS3} > 0$ wide range of input current Iin2.We literature survey we can find the most suitable operation mode of M5 is sub threshold region because here low input current and in saturation region high input current of M1 and M3. The assumption under the $V_{DS5} > 3Vt$, the sub-threshold drain current of transistor M5 can be expressed by

$$I_{bias2=}\frac{W5}{L5}\ I_{DO5}\ \exp\left(\frac{V_{SG5-|Vtp|}}{nV_T}\right) \quad (4.1)$$

In above equation (4.1) W5 and L5 represent the channel width and length of transistor M5, and V_T (approximately ≈26mv at room temperature) [2] is thermal voltage. The Constant n and I_{DO5} are process parameters. Typically, value of I_{DO5} ≈20 nA and n lie between 1.2 and 2.0 [2]. For the sub-threshold operation of transistor M5 $V_{SG5\approx|Vtp|}$ and saturation operation of transistor M1 and M3, find

$$I_{in2} \leq \frac{kA_C\ V_{SG5}^2}{2} \leq \frac{kA_C\ V_{tn}^2}{2} \quad (4.2)$$

When transistors M1, M3, M5 are in sub-threshold region, and the gate to source voltage of M1, M3 and M5 are almost near to their threshold voltages, can find

$$I_{in2} \leq \frac{W1 I_{DO1}}{L1} \quad (4.3)$$

$$V_{in2} = nV_T \ln \frac{I_{in2}}{I_{DO1}}\ \frac{L1}{W1} + V_{tn} \leq V_{tn} \quad (4.4)$$

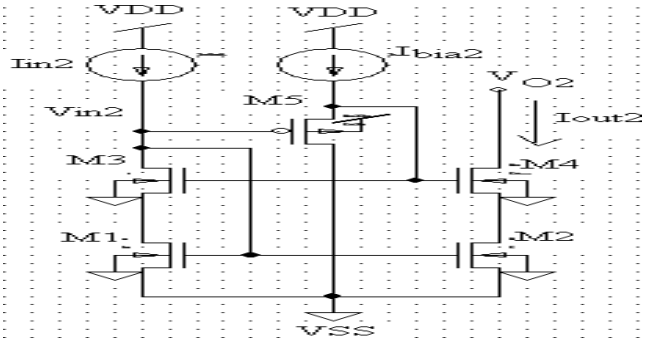

Figure 4.1 Level Shifted Low Voltage CascadeCurrent Mirror

$$V_{O2,min} = V_{GS2} + V_{GS4} - 2V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} + \sqrt{\frac{2I_{in}}{KA_C}} \quad (4.5)$$

5. SIMULATION RESULTS

5.1 INPUT CHARACTERISTICS OF LOW VOLTAGE CMOS CURRENT MIRROR

The circuit shown in figure 2.1 is simulated using 0.18µm IBM model parameters with supply voltage

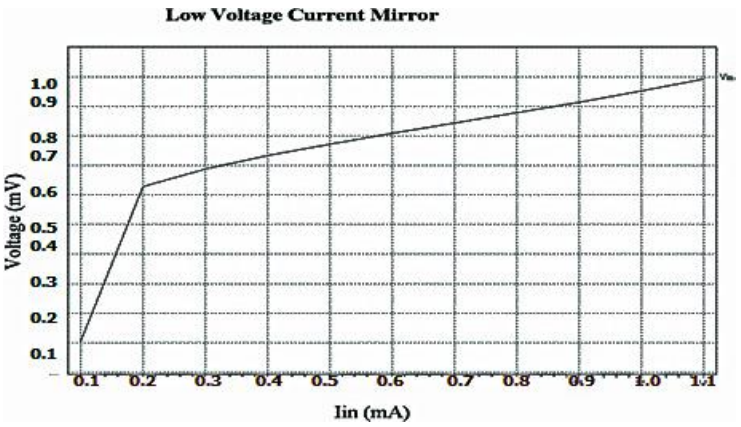

Figure 5.1 Input characteristics LVCM

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of 1V. The purpose was to obtain a high performance LVCM that have high input and output voltage swing capabilities. Table 5.1 summarizes the (W/L) ratios of MOSFETs used in circuits. In figure 5.1 Vin is input voltage and Iin is input current and shows input voltage V_{in} requirement for various values of input current I_{in}. V_{in} Required is 0.51V for low voltage current mirror structures at I_{out} of 1mA.

5.2 CURRENT TRANSFER CHARACTERISTICS OF LOW VOLTAGE CURRENT MIRROR

Figure 5.2 shows current transfer characteristics of low voltage current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M3) of transistor M3 is input or reference current and drain current id(M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

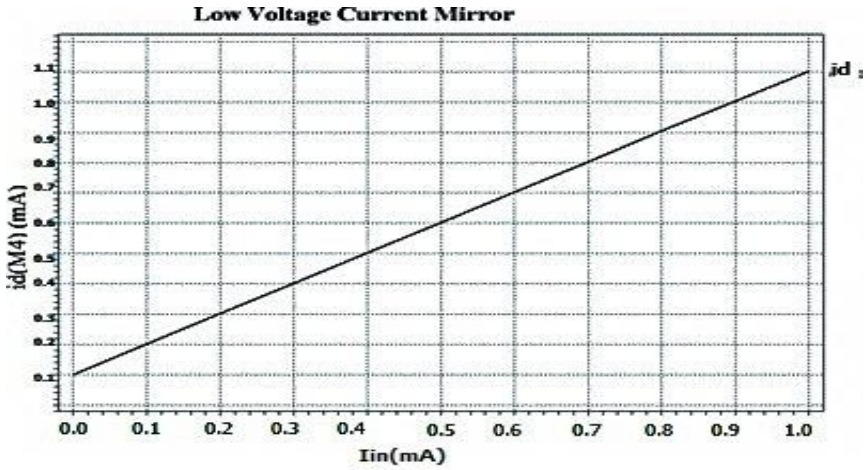

Figure 5.2 Current transfer characteristics LVCM

5.3 POWER DISSIPATION RESULTS FOR LOW VOLTAGE CURRENT MIRRROR

Low voltage current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 1000µA. Width and length of transistors (M3 & M4 and M1 & M2) are kept same. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 5.3 shows power dissipation results. Power results are reported at the end of transient simulation in the output file

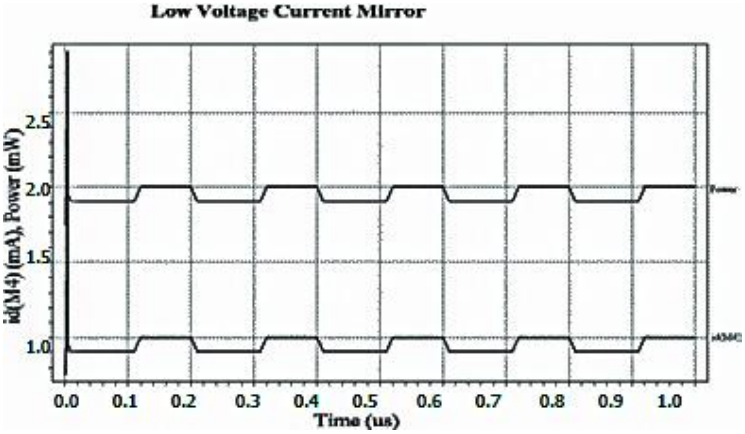

Figure 5.3 Power dissipation of LVCM

POWER RESULTS

v3 from time 0 to 2e-007

Average power consumed -> 1.953325e-003 watts

Max power 2.908787e-003 at time 4.19717e-009

Min power 1.749169e-003 at time 0

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5.4 FREQUENCY RESPONSE OF LOW VOLTAGE CURRENT MIRROR

The frequency response of low voltage current mirror is shown in figure 5.4. The frequency response of cascade current mirror is dependent on the capacitive load (Cload). In figure 5.4 the -3db bandwidth is 240Mhz for a load capacitance of 10 pF.

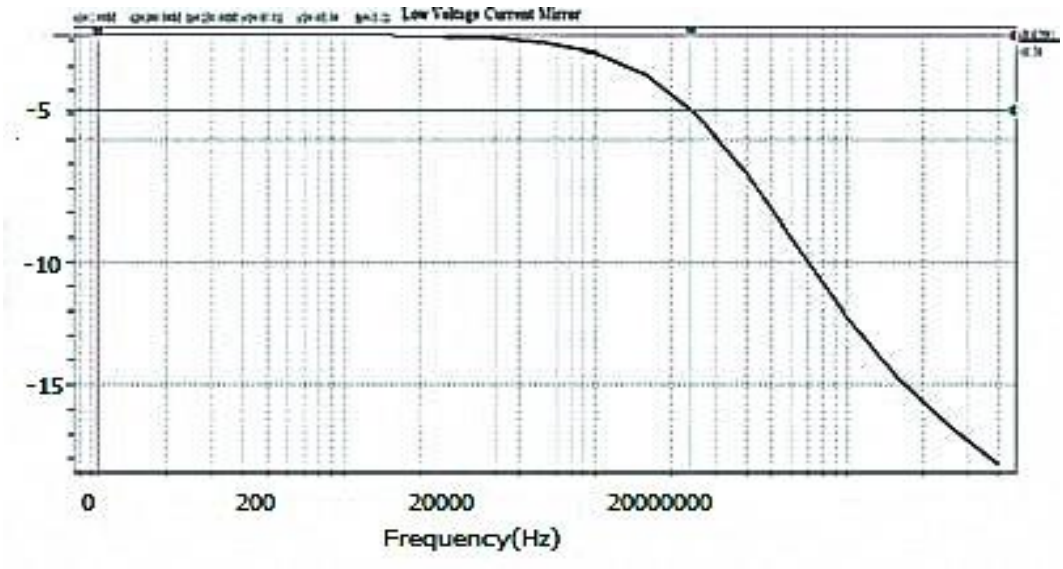

Figure 5.4 Bandwidth of Low Voltage CurrentMirror

5.5 DYNAMIC RANGE CALCULATION OF LOW VOLTAGE CURRENT MIRROR(LVCM)

Table 5.1: Aspect Ratio of transistors used inin lowvoltage current mirror.

MOSFETs	Type	Width	Length
M1,M2,M3,M4	NMOS	20µm	0.5µm
M5	PMOS	10µm	0.3µm

Table 5.2: Parameters used in Low VoltageCurrent Mirror (LVCM)

Parameter	Unit
Supply voltage	1.0 volt
V_{bias} **(Voltage bias)**	-0.2 volt
Threshold voltage V_{tn} **(NMOS)**	0.44 Volt
Transconductance	156.8µA

5.6 MAXIMUM INPUT CURRENT RANGE CALCULATION FOR LOW VOLTAGE CURRENT MIRROR

Equation (2.7) discuss the concept of maximum range of low voltage current mirror. In $I_{in,max}$ equation, K is the transconductance ,A_M is the aspect ratio of M1 and M2 transistors and A_C is the aspect ratio of M3 and M4 transistors. V_B is the biasing voltage, V_{tn} is the threshold voltage.

$$I_{in,max} = \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2$$

$$I_{in,max} = \frac{156.8}{2} \times 40 (-0.2 - 0.44)^2 \left(\frac{\sqrt{40/40}}{1+\sqrt{40/40}}\right)^2$$

$$= \frac{156.8}{2} \times 40 (-0.2 - 0.44)^2 \left(\frac{\sqrt{1}}{1+\sqrt{1}}\right)^2$$

$$= \frac{156.8}{2} \times 40 (-0.2 - 0.44)^2 \times \left(\frac{1}{2}\right)$$

$$= \frac{156.8}{2} \times 40 (-0.64)^2 \times \left(\frac{1}{2}\right)$$

$$= 642.88\mu A$$

$$= 0.64mA$$

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As discussed above, in low voltage current mirror all transistors are identical and operate in saturation region, saturation region operation condition is given by $V_{DS}= V_{GS} -V_{tn}$

For low voltage current mirror design in 0.18µm technology,

$V_{DS}=V_{GS} -V_{tn}$,V_{DS}=1.20-0.44 ,V_{DS}=760Mv, I_{in}=0.64 mA

Transistor M3 and M4 gate voltage (V_{GS})

$V_{DS}=V_{GS} -V_{tn}$, 760= V_{GS} -440, VGS=1200=1.20v

The figure 5.5 shows maximum input current of low voltage current mirror here input current is sweep 0mA to 5 mA with supply voltage 1V. In figure 2.1 we discuss the low voltage current mirror below shows the waveform when Iin increases the drain voltage of M1 transistor decrease shows the waveform and maximum input current find the above equation through find value and plot the waveform.

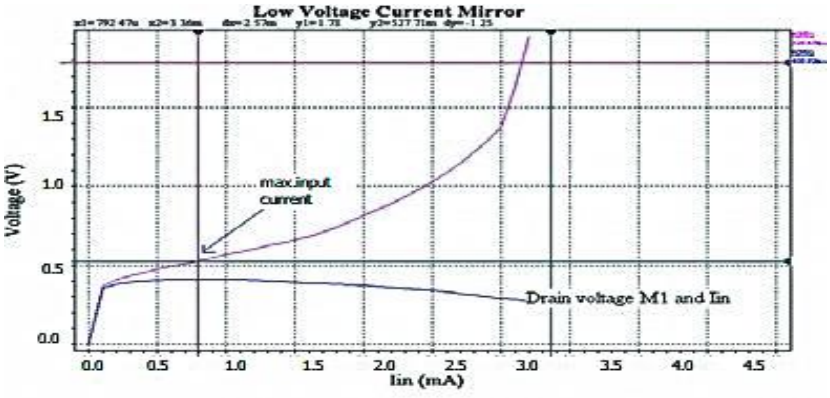

Figure 5.5 Low voltage current mirrormaximum input current

5.7 MINIMUM INPUT CURRENT RANGE CALCULATION FOR LOW VOLTAGE CURRENT MIRROR

Equation (2.8) discuss the concept of minimum input current range for low voltage current mirror. Below we have calculated the minimum input current range according to design specifications.

$I_{in,\,max} = \frac{K}{2} A_M (V_{BC} - Vtn)^2$

$I_{in,max} = \frac{156.8}{2} (-0.2-1\times0.44)^2 \times 40 = 78.4\times1.17\times40 = 0.37$ mA

Figure 5.6 shows drain voltages of M1 & M3 transistors for a Iin sweep from 5µA to 5mA.

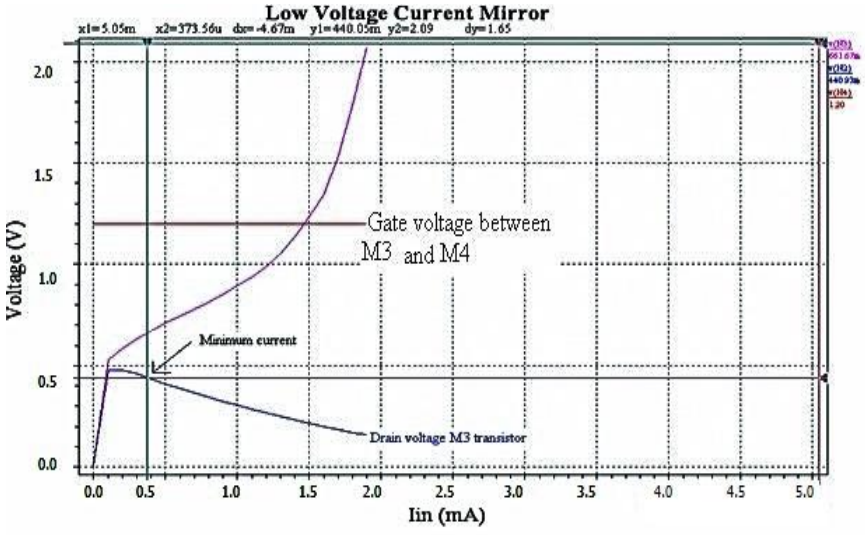

Figure 5.6 Low voltage current mirror minimuminput current

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5.8 Input Characteristics of Level Shifted Low Voltage Cascade Current Mirror

The circuit shown in figure 4.1 is simulated using 0.18µm IBM model parameters with supply voltage of 1V. The purpose was to obtain a high performance LVCM that have high input and output voltage swing capabilities. Table 5.1 summarizes the (W/L) ratios of MOSFETs used in circuits. In figure 5.7, V_{in} is input voltage and Iin is input current and shows input voltage V_{in} requirement for various values of input current I_{in}. V_{in}. Required is 0.51V for low voltage level shifted cascade current mirror structures at I_{out} of 1mA.

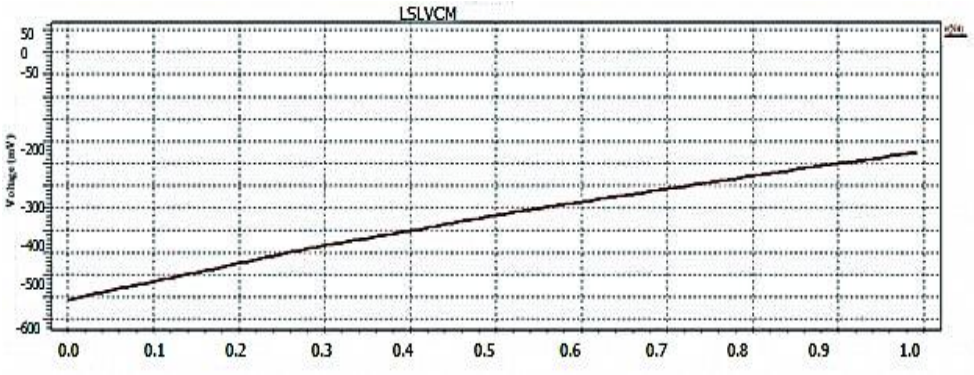

Figure 5.7 Input characteristics LSLVCM

5.9 CURRENT TRANSFER CHARACTERISTICS OF LEVEL SHIFTED LOW VOLTAGE CASCADE CM

Figure 5.8 shows current transfer characteristics of level shifted low voltage current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M3) of transistor M3 is input or reference current and drain current id (M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current. output current very from 1µA to 1mA. Figure 5.9 shows improved dynamic range current transfer characteristics of level shifted low voltage current mirror and output current very from 1µA to 2mA.

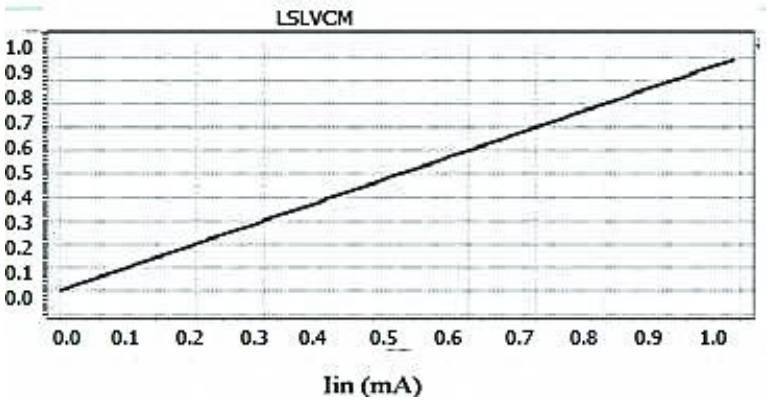

Figure 5.8 Current transfer characteristics of LSLVCM

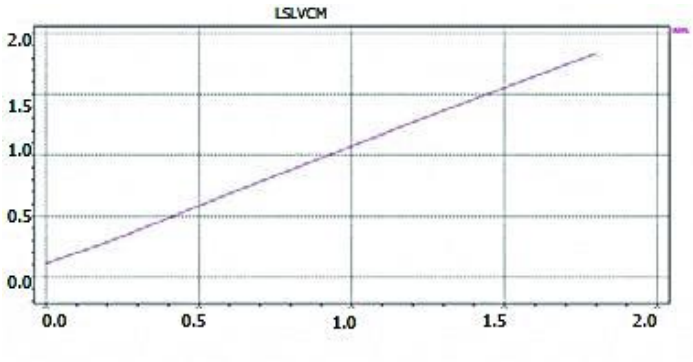

Figure 5.9 Current transfer characteristics of LSLVCM

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5.10 FREQUENCY RESPONSE OF LEVEL SHIFTED LOW VOLTAGE CASCADE CURRENT MIRROR

The frequency response of level shifted low voltage current mirror is shown in figure 5.10 The frequency response of LSLVCM is dependent on the capacitive load (Cload). In figure 5.10 the - 3db bandwidth is 887.83Mhz for a load capacitance of 50 pF

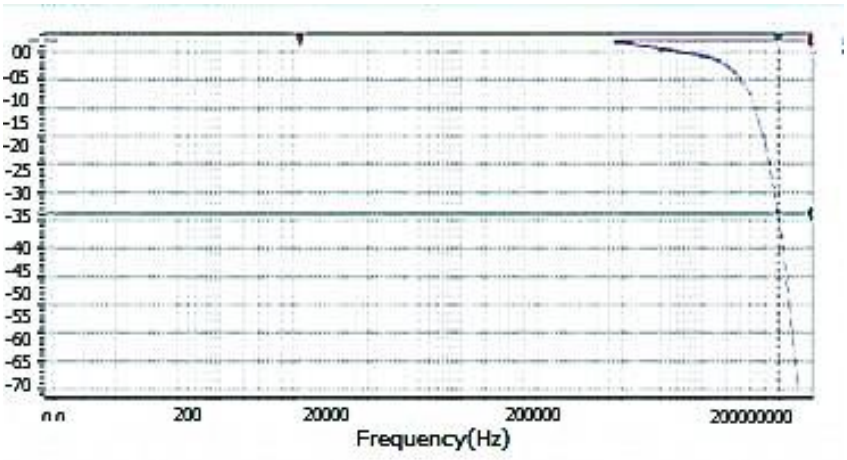

Figure 5.10 Bandwidth of Level Shifted LowVoltage Current Mirror

5.11 POWER DISSIPATION RESULTS FOR LEVEL SHIFTED LOW VOLTAGE CURRENT MIRRROR

Level shifted low voltage current mirror circuit is simulated using 0.18µm IBM MOS modelparameters with supply voltage 1.0 V and I_{in} of 1mA. Width and length of transistors (M3 & M4 and M1 & M2) are kept same. Transient analysis isused to calculate the power dissipation in the current mirror. Figure 5.11 shows power dissipation results. Power results are reported at theend of transient simulation in the output file.

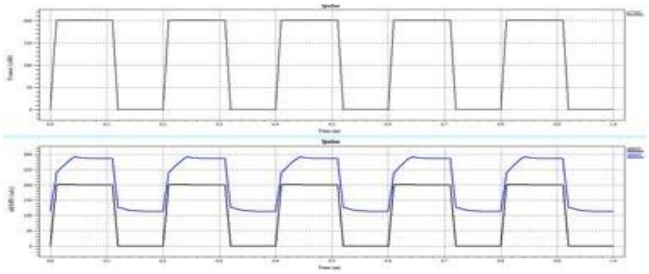

Figure 5.11 Power dissipation of LSLVCM

5.12 OUTPUT CHARACTERISTICS OFLEVEL SHIFTED LOW VOLTAGECURRENT MIRROR AT HIGH CURRENTS

Low voltage current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 5.12 shows the output current characteristics at high current at different – different input current value. In waveform shows the characteristic O 0 mA to 2 mA and supply voltage is 1mV .

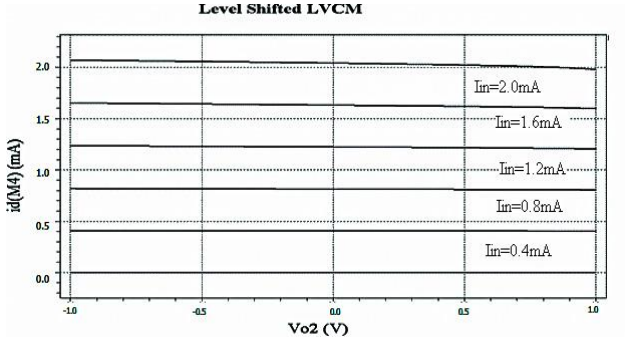

Figure 5.12 Output Current Characteristics at High Currents

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5.13 OUTPUT CHARACTERISTICS OF LEVEL SHIFTED LOW VOLTAGE CURRENT MIRROR AT LOW CURRENTS

Level shifted low voltage current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 5.13 shows the output current characteristics at low current at different – different input current value. In waveform shows the characteristics Iin 0µA to 100µA and supply voltage 1V.

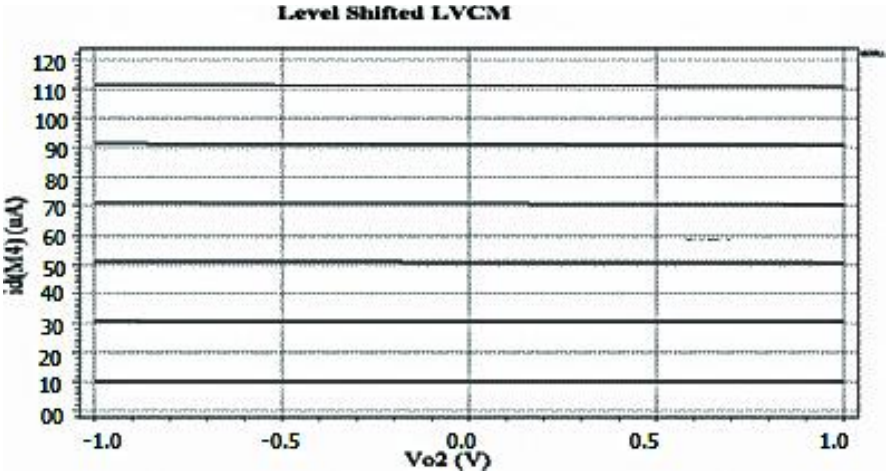

Figure 5.13 Output Current Characteristics at Low Currents

6. CONCLUSION

In this paper the low voltage CMOS cascade current mirror is designed using IBM 0.18µm technology with a supply voltage of 1.0 volt. The simulated results for different low power current mirror topologies show significant low power dissipation with enhanced dynamic rangeand improved bandwidth. The simulated designs can be used in high performance analog and mixed mode Very Large-Scale Integration circuits especially for active elements like as op-amps, current conveyors, current feedback amplifiers etc.

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